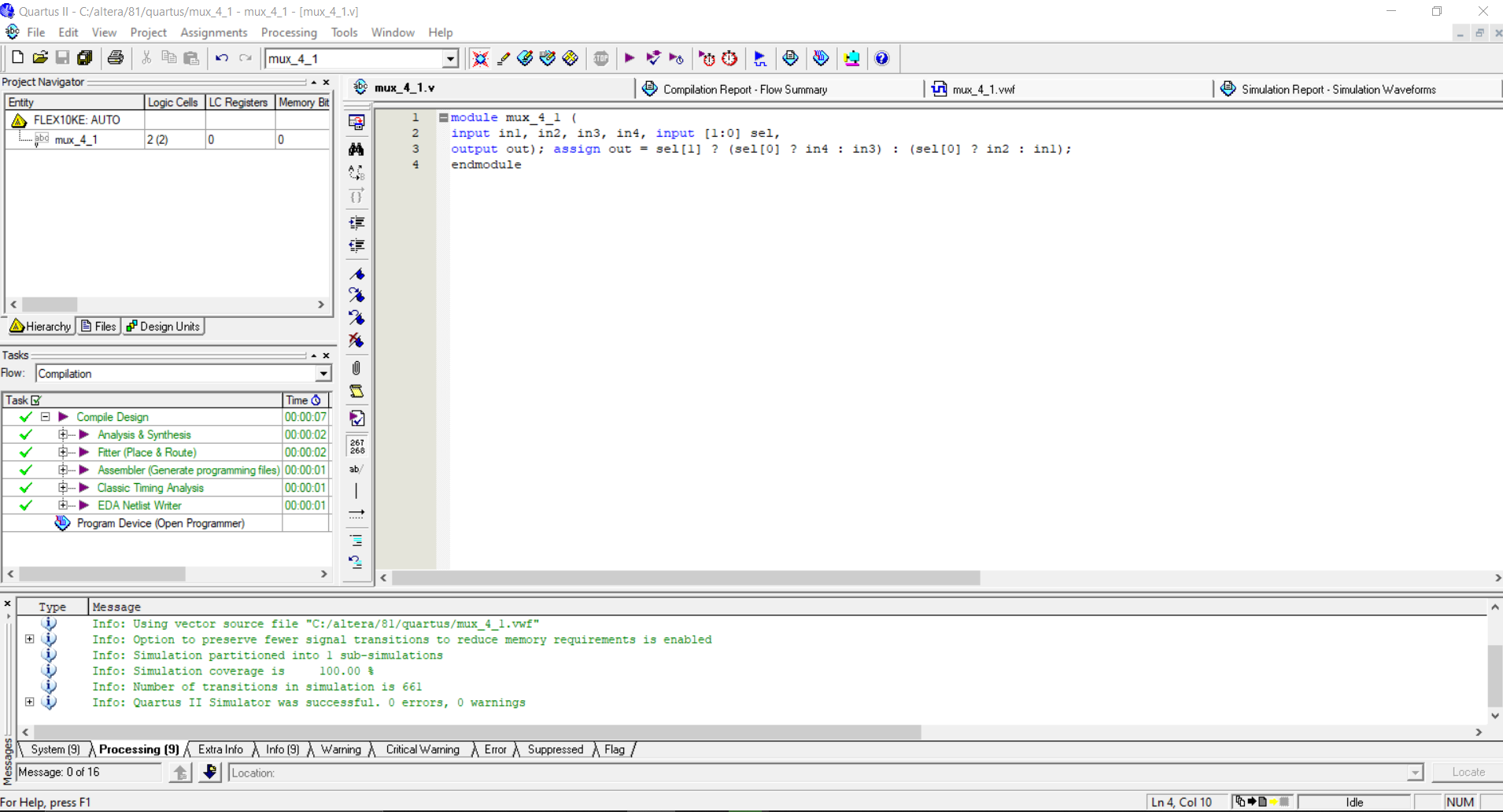
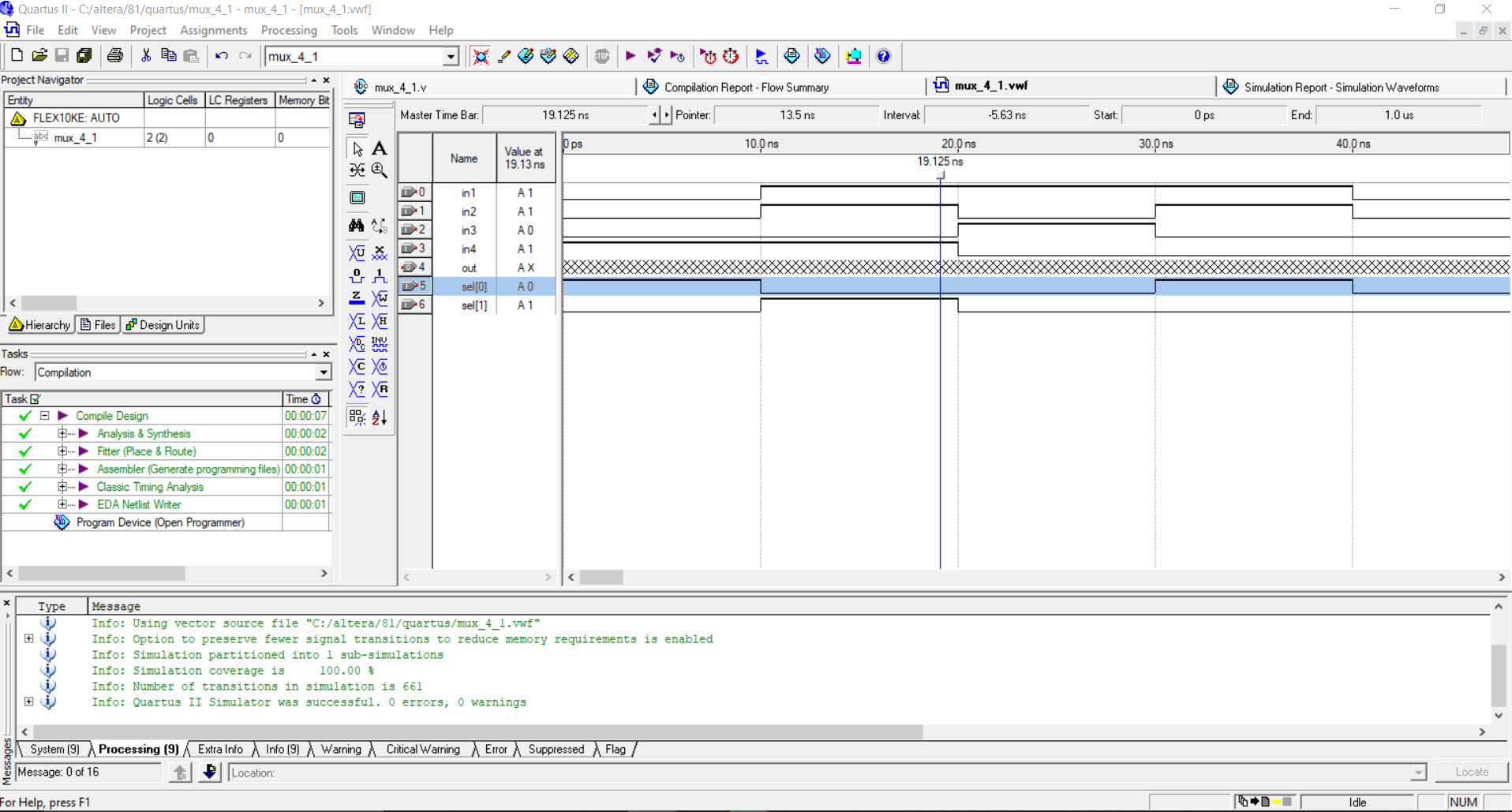
1. Design a 4 to 1 MUX using Verilog HDL & verify using timing diagram

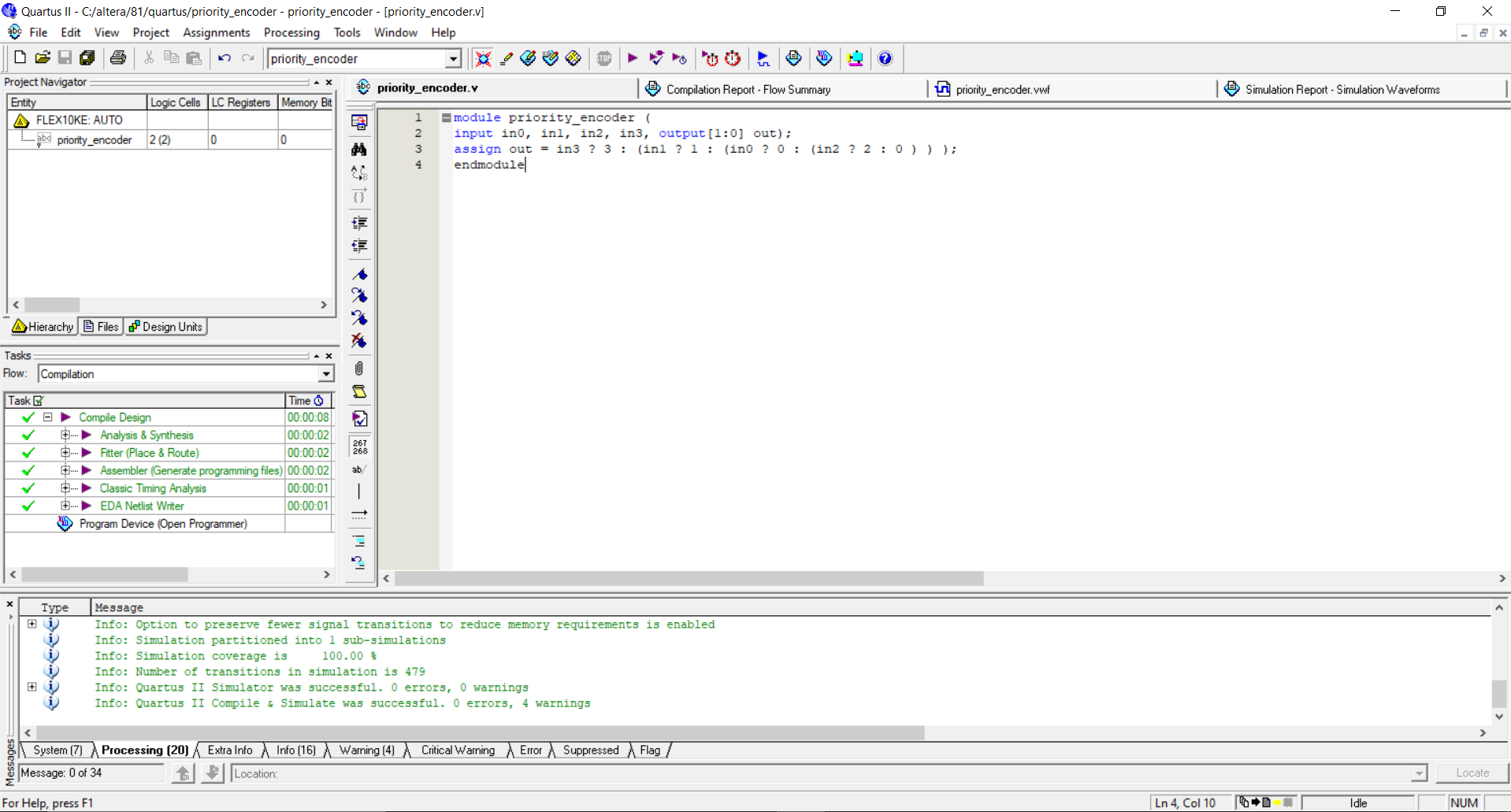
**Code**:

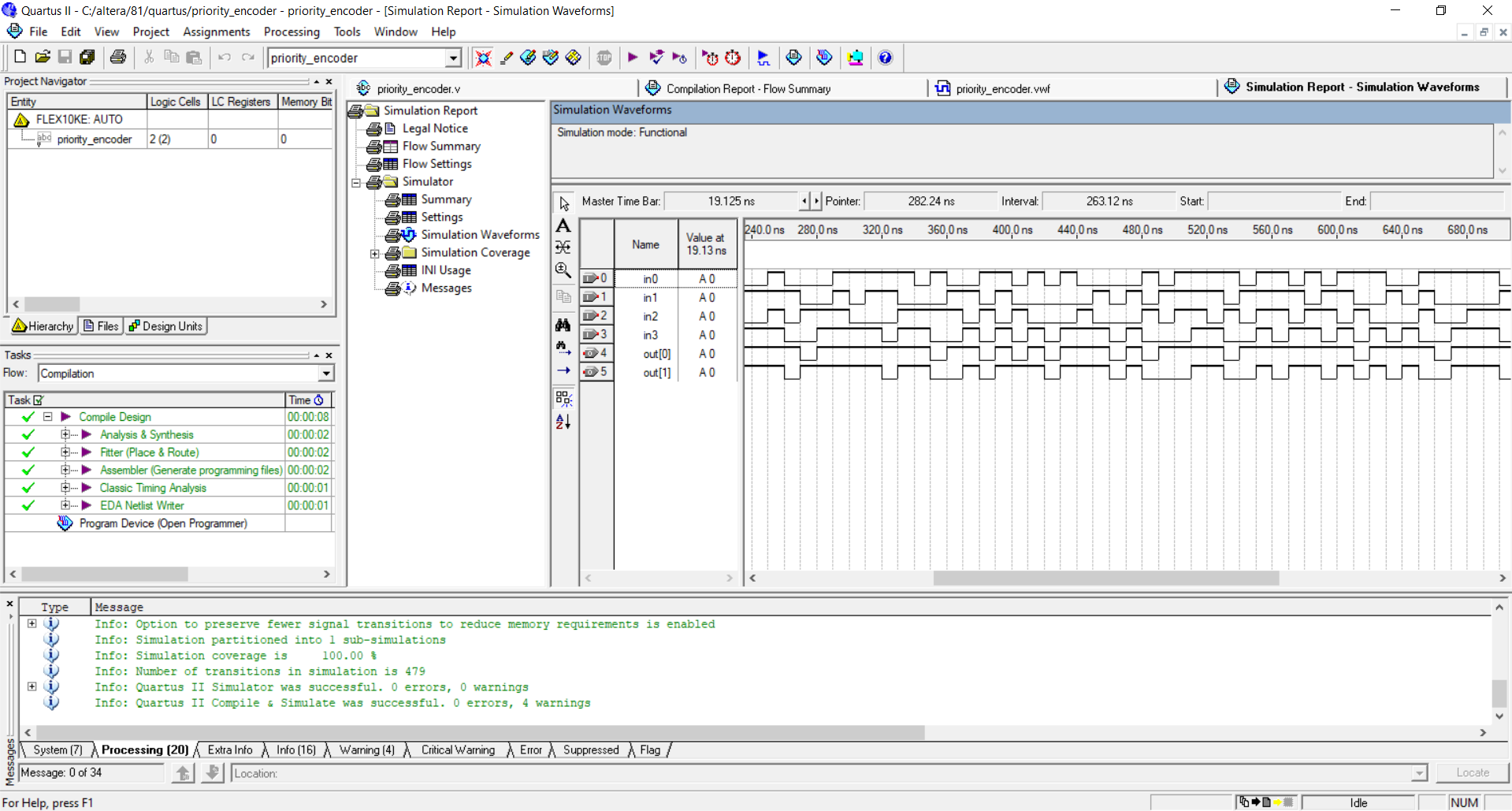




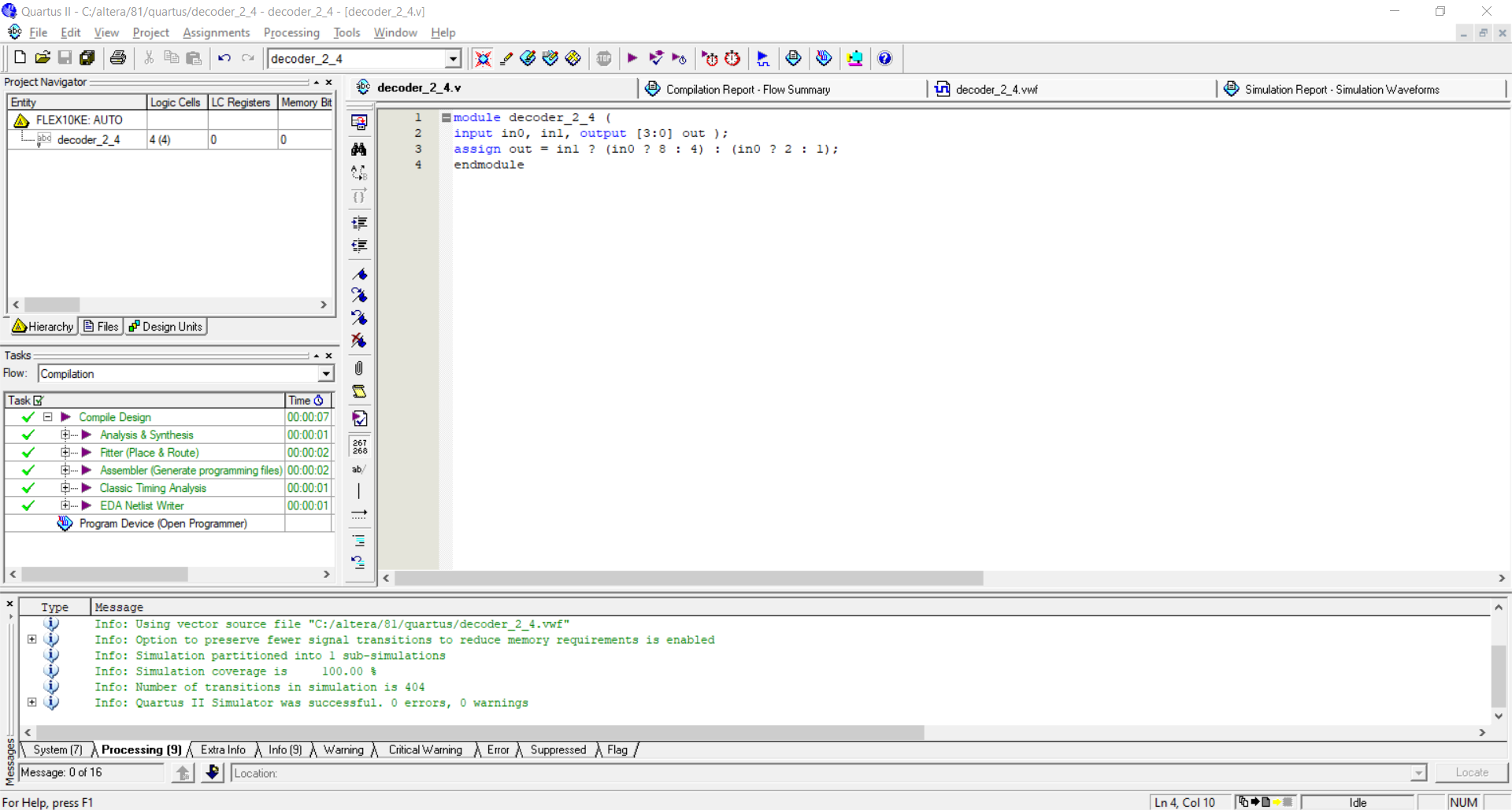
2. Design a priority encoder (3>1>0>2) using Verilog HDL and verify using timing diagram.

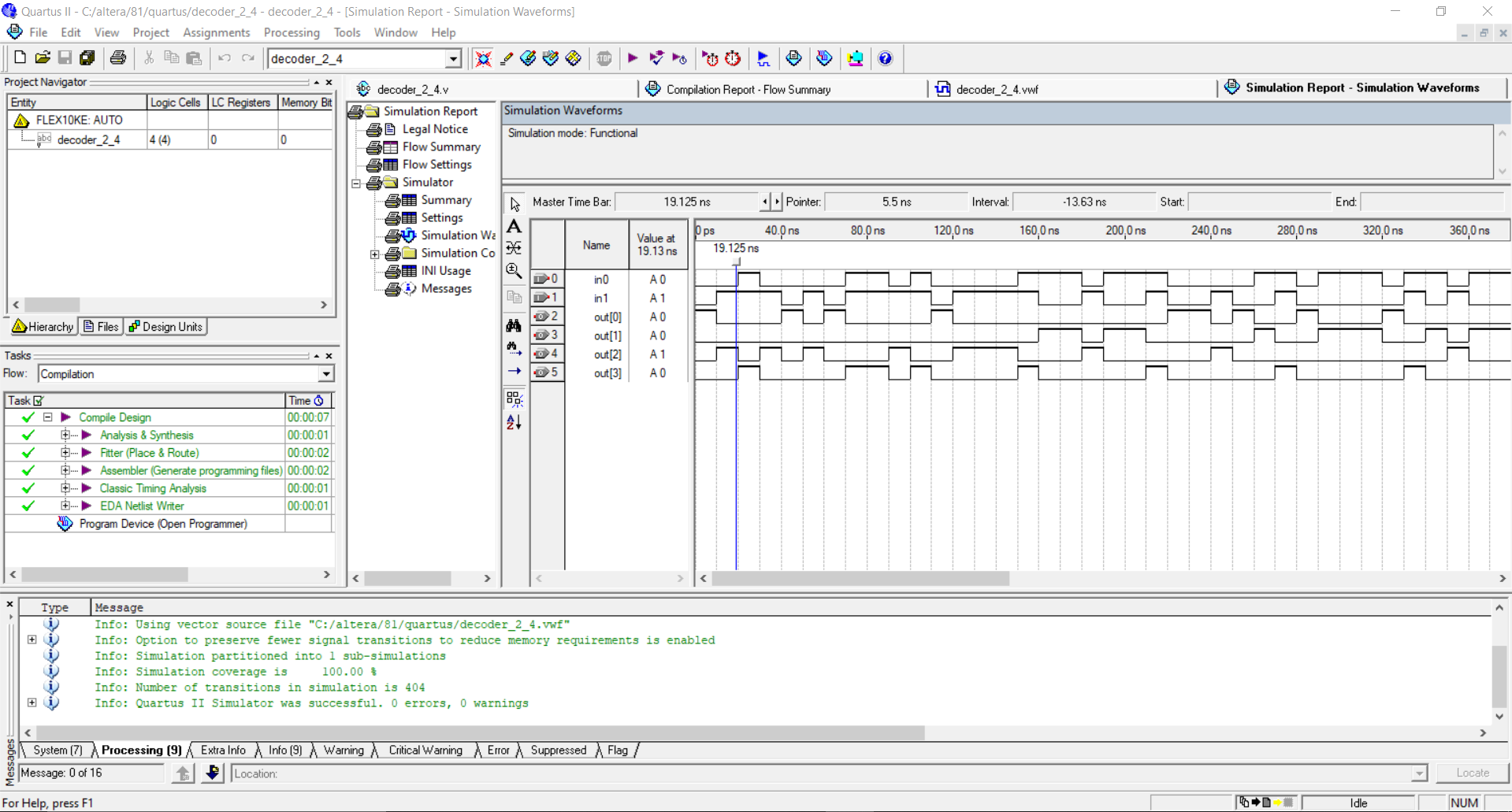
**Code:**





Code 3





Code 4 :

